(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 089 331 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
04.04.2001 Bulletin 2001/14

(51) Int Cl.[7]: **H01L 21/60**, H01L 23/485

(21) Application number: **00126587.5**

(22) Date of filing: **18.12.1990**

(84) Designated Contracting States:
AT BE CH DE DK ES FR GB GR IT LI LU NL SE

(30) Priority: **18.12.1989 US 452191**

(62) Document number(s) of the earlier application(s) in accordance with Art. 76 EPC:
95114886.5 / 0 690 490
91902599.9 / 0 506 859

(71) Applicant: **PFC Corporation**
Billerica, MA 01821 (US)

(72) Inventors:
- **Estes, Richard H.**
Pelham, NH 03076 (US)
- **Kulesza, Frank W.**
Winchester, MA 10890 (US)

(74) Representative: **Hess, Peter K., Dipl.-Phys.**
Bardehle,Pagenberg,Dost,Altenburg,Geissler,Isenbruck
Patent- und Rechtsanwälte
Postfach 86 06 20
81633 München (DE)

Remarks:
This application was filed on 13 - 12 - 2000 as a divisional application to the application mentioned under INID code 62.

(54) Flip chip technology using electrically conductive polymers and dieletrics

(57) A method is presented for interconnecting bond pads of a flip chip with bond pads of a substrate by an electrically conductive polymer. An organic protective layer is selectively formed over a surface of a flip chip to thereby leave exposed bond pads on the flip chip. An electrically conductive polymerizable precursor is disposed on the bond pads extending to a level beyond the organic protective layer to thereby form bumps. The bumps are aligned with bond pads of a substrate and then contacted to those bond pads. The bumps can be polymerized either before or after contacting the bumps to the bond pads of the substrate to form electrically conductive interconnections between the bond pads of the flip chip and the bond pads of the substrate.

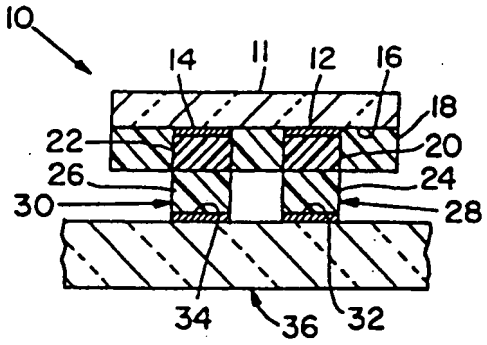


Fig. 8

EP 1 089 331 A2

Description

[0001] Integrated circuits have had almost universal application to communication and military technologies for several years. Of increasing importance has been development of microcircuit wafers and methods for interconnection of the circuits by automated equipment. A primary limitation to application of microcircuit technology has been cost efficiency and reliability of interconnection of integrated circuits on chips because of the small size of the chips, which often require hundreds of connections to be made within each circuit.

[0002] One method of circuit interconnection is called flip chip bonding. Flip chip bonding can offer a shorter signal path and, therefore, more rapid communication between circuits than can other methods, such as tape automated bonding (TAB) or conventional wire bonding, because bond pads on flip chips are not restricted to the periphery of the chip, but rather are usually located at one face of the chip opposite a substrate. In one method of flip chip bonding, a chip or die is formed with the requisite integrated circuit and interconnect wiring required for interconnecting the circuit with other chip circuits on a circuit board, such as a separate printed circuit board or substrate. Bond pads are located at points of interconnection. Bumps are formed by plating of several layers of metals on the bond pads of the flip chip. Following deposition, the chip is heated to reflow the metals, thus causing surface tension of the deposit to form hemispherical solder "bumps." The flip chip is subsequently severed from the wafer of which it was a part and "flipped" for alignment with the bond pads of a substrate. These bumps are then contacted with the bond pads of the substrate and uniformly heated to simultaneously form interconnects between aligned bond pads of the flip chip and the substrate.

[0003] Use of metals to interconnect bond pads of flip chips and substrates has required, however, that passivation of the flip chip be accomplished by use of a metal barrier such as titanium (Ti), tungsten (W) or silicon nitride (Si_3N_4). Both the metal, as a passivation (or barrier) material, and ceramic, as a substrate material, are generally necessitated to allow sufficient heating to enable reflow of the solder bumps for interconnection between the flip chip and the substrate without consequential damage to either.

[0004] Fabrication of circuits using bumped flip chips have also been limited by the inability to visually inspect interconnections between the flip chip and the substrate. Further, the yield of finished mounted circuits can be detrimentally affected by failure of interconnects caused by the difference between the coefficients of thermal expansion of the various materials comprising the flip chip, the passivation layer, the solder bumps and the substrate. Also, melting of the solder bumps creates an electrically conductive flux as an undesirable byproduct which generally must be removed from between the substrate and the flip chip to allow proper operation of the finished circuit.

[0005] Problems of heat stress during fabrication have been addressed by various methods, such as by rapid application of heat to a bumped flip chip and rapid conduction of heat from the solder interconnects in order to minimize damage to flip chips, substrates and interconnections due to internal stresses caused by thermal expansion and contraction. However, this method is very expensive.

[0006] Therefore, a need exists for a method of interconnecting flip chips to substrates which is fast, cost-effective and reliable, so that the advantages of flip chips over other types of microcircuit wafers can be exploited more fully. Also, there is a demand for a simplified method of connecting flip chips to substrates which eliminates the need for elaborate plating procedures. Further, a method which enables greater flexibility of passivation and choice of substrate is also desirable. These improvements could promote cost efficiency and broaden the applications for which microcircuits are suitable.

Summary of the Invention

[0007] The present invention relates to a bumped flip chip technology and a method for interconnecting the bond pads of a bumped flip chip to the bond pads of a substrate. In accordance with the present invention, an organic protective layer is selectively formed over the surface of a flip chip, leaving the flip chip bond pads exposed. An electrically conductive polymerizable precursor is disposed at the bond pads of the flip chips to form "bumps" which extend beyond the organic protective layer. Alternatively, the electrically conductive polymerizable precursor can be formed in two layers at each bond pad, the two layers together forming the bumps. The two layers can be polymerized to form an electrically conductive bump before connecting the bump with bond pads of the substrate. An adhesive is then applied to the substrate bond pads to provide "wet," or electrically conductive, connections between the bumps and substrate which are subsequently polymerized. An electrically conductive polymer is thereby selectively i formed between the bond pads of the flip chip and the bond pads of the substrate. Alternatively, the bumps can be polymerized after connecting the bumps of the flip chip to the bond pads of the substrate.

[0008] Electrical interconnections between bond pads of flip chips and bond pads of substrates are obtained by formation of a electrically conductive polymerizable precursor at the bond pads of a flip chip. Polymerization of the bumps can be achieved under milder thermal conditions than are required to reflow solder. Thus, reliability problems, caused by rapid heating and by large discrepancies of coefficients of thermal expansion of component materials in the flip chip, passivation layer, bumps and substrates, can be substantially reduced. Further, because the polymerization conditions are less harsh than required for reflow of solder bumps,

the need for metal passivation of the flip chip is eliminated and a wider variety of substrate types is enabled. Also, complicated and time-consuming vapor deposition and electroplating techniques for depositing solder bumps are eliminated. In addition, polymer interconnects are fluxless, thus eliminating difficult problems with removal of electrically conductive flux between flip chips and substrates. The organic protective layer can also have a low dielectric constant, thereby acting as a passivation layer and enabling close proximity of the flip chip to the substrate and consequent shortened circuit paths in the finished circuit.

[0009] The above features and other details of the invention, either as steps of the invention or as combinations of parts of the invention, will now be more particularly described with reference to the accompanying drawings and pointed out in the claims. It will be understood that the particular embodiments of the invention are shown by way of illustration and not as a limitation of the invention. The principle feature of the invention may be employed in various embodiments without departing from the scope of the invention.

Detailed Description of the Drawings

[0010] Figure 1 is a plan view of one embodiment of the present invention after selective formation of an organic protective layer over the surface of a flip chip.

[0011] Figure 2 is a section view of the embodiment of Figure 1 taken along lines I-I.

[0012] Figure 3 is a section view of a flip chip which has been passivated with a silicon nitride or oxide layer, over which layer an organic protective layer has been formed.

[0013] Figure 4 is a section view of the embodiment of Figure 1 after formation of the first layer of an electrically conductive polymerizable precursor on the bond pads of the flip chip.

[0014] Figure 5 is a section view of the embodiment of Figure 1 after formation of a second layer of an electrically conductive polymerizable precursor on the first layer to thereby form bumps.

[0015] Figure 6 is a plan view of a substrate suitable for use with the present invention.

[0016] Figure 7 is a section view of the embodiment of Figure 1 and of the substrate taken along lines VI-VI of Figure 6 after aligning the bumps of the flip chip with bond pads of the substrate.

[0017] Figure 8 is a section view of the embodiment of Figure 1 after contact of the bumps of the flip chip to the bond pads of the substrate.

[0018] Figure 9 is a section view of a third embodiment of the present invention wherein the bumps have been polymerized to form an electrically conductive polymer and wherein an electrically conductive adhesive has been applied to the substrate bond pads prior to contacting the flip chip bumps to the bond pads of the substrate.

[0019] Figure 10 is a section view of the embodiment of Figure 9 after contacting the bumps to the bond pads of the substrate and polymerization of the adhesive to form electrical interconnections between the bond pads of the flip chip and the bond pads of the substrate.

Detailed Description of the Invention

[0020] In one embodiment of the present invention, shown in Figure 1, a simplified illustrative version of a flip chip 10 is shown. It consists of bond pads 12,14 on upper planar surface 16 of flip chip die 11. Die 11 is formed of silicon, gallium arsenide, germanium or some other conventional semiconductor material. As can be seen in Figure 2, an organic protective layer 18 is formed over circuits 15 (connected to the bond pads) and surface 16 of flip chip 10 by screen printing, stenciling, spin-etching or by other methods of monomer or polymer deposition. Alternatively, flip chip 10 also can be passivated with silicon nitride or an oxide layer 19 before formation of organic protective layer 18, as is shown in Figure 3. The organic protective layer is preferably a dielectric polymer. An example of an organic material suitable for application in the present invention is Epo-Tek^{R} polyimide, manufactured by Epoxy Technology, Inc. Bond pads 12,14 are covered during deposition of organic protective layer 18 and are then left exposed following deposition, as shown in Figure 2. Organic protective layer 18 is preferably polymerized by application of heat or other conventional means prior to formation of layers 20,22 on bond pads 12,14, shown in Figure 4. Organic protective layer 18 passivates and thereby insulates and protects the underlying surface 16 of flip chip 10.

[0021] As shown in Figure 4, first layers 20,22 of an electrically conductive polymerizable precursor are selectively formed on bond pads 12,14. Electrically conductive polymerizable precursor, as that term is used herein, can include a thermoset polymer, a B-stage polymer, a thermoplastic polymer, or any monomer or polymer which, upon polymerization or upon further polymerization, is electrically conductive or which can support an electrically conductive material. The electrically conductive polymerizable precursor can be gold-filled, silver-filled, or filled with some other electrically conductive material. The organic protective layer 18 acts as a template defining areas for deposition of first layers 20,22 of monomer on flip chip 10. In a preferred embodiment of the present invention, the unpolymerized organic protective layer has a high thixotropy for retaining a pattern on surface 16. The flip chip 10 can thus be manipulated more conveniently during subsequent deposition of electrically conductive polymerizable precursor onto bond pads 12,14. First layers 20,22 are substantially flush with polyimide layer 18. Second layers 24,26 of electrically conductive polymerizable precursor, such as are used to form first layers 20,22, are formed on first layers 20,22, as shown in Figure 5. First

layers 20,22 and second layers 24,26 form bumps 28,30 on flip chip 10. As shown in Figure 6, circuit 33 on substrate 36 is connected with bond pads 32,34. As can be seen in Figure 7, bumps 28,30 are located on flip chip 10 in a position which is aligned with the known position of bond pads 32,34 on substrate 36. As shown in Figure 8, bond pads 32,34 are then brought into contact with bumps 28,30. Bumps 28,30 are then polymerized by heating, or by other known methods, to form electrically conductive interconnections between flip chip bond pads 12,14 and substrate bond pads 32,34. Substrates which are suitable for use with the present invention include materials such as ceramic, silican, porcelain, conventional printed circuit board materials, or other conventional substrates suitable for electrical circuits.

[0022] If the electrically conductive polymerizable precursor is a thermoset, the first layers 20,22 can be polymerized before formation of the second layers 24,26. Second layers 24,26 can be hemispherical in shape before contact is made with substrate bond pads 32, 34. First layers 20,22 and second layers 24,26 form bumps 28,30 which can be contacted to substrate bond pads 32,34 before polymerization. Bumps 28,30 are subsequently polymerized to form electrical interconnections between flip chip bond pads 12,14 and substrate bond pads 32,34. Alternatively, first layers 20,22 can be polymerized before deposition of second layers 24,26.

[0023] In another embodiment of the present invention, shown in Figure 9, bumps 28,30 can be formed of electrically conductive polymerizable precursor which is polymerized before contact with substrate bond pads 32,34. As seen in Figure 9, adhesive layers 38,40 are formed on substrate bond pads 32,24 before bumps 28,30 are contacted to substrate bond pads 32,34. Examples of adhesives which can be used include thermosets, thermoplastics and polymer thick film. Adhesive layers 38, 40 are formed on substrate bond pads 32, 34 by screen printing, stenciling, or by some other conventional method. Bumps 28,30 are brought into contact with adhesive layers 38, 40 are shown in Figure 10, and the electrically conductive adhesive is then polymerized by heating or by other conventional means to form electrical interconnections between bond pads 12,14 of flip chip 10 and bond pads 32,34 of substrate 36.

[0024] The electrically conductive polymerizable precursor used to form first layers 20,22 and second layers 24,26 of bumps 28,30 can be a B-stage polymer. Examples of suitable B-stage polymers include thermosets and thermoplastics. Solvents within the B-stage polymer can be substantially evaporated from the electrically conductive polymerizable precursor comprising bumps 28,30 before bumps 28,30 are contacted to substrate bond pads 32,34. Evaporation of the solvent within the B-stage polymer causes the bumps 28,30 to retain a substantially rigid shape while the flip chip is manipulated for contacting bumps 28,30 to substrate 36. The B-stage polymer can subsequently be polymerized to form electrical interconnections between flip chip bond pads 12,14 and substrate bond pads 32,34.

[0025] In a preferred embodiment, flip chip 11 is aligned over substrate 36 by a flip chip aligner bonder, such as model M-8, manufactured by Research Devices, Division of the American Optical Corporation.

Equivalents

[0026] Although preferred embodiments have been specifically described and illustrated herein, it will be appreciated that many modifications and variations of the present invention are possible, in light of the above teachings, within the purview of the following claims, without departing from the spirit and scope of the invention. For example, while the discussion is directed to a single flip chip on a substrate which flip chip has only one circuit and two bond pads, it is to be understood that the concept can be readily expanded to include a plurality of chips with a plurality of circuits and bond pads on each.

Claims

1. A method of forming an electrically conductive interconnection between a bond pad (12, 14) of a flip chip (10) and a bond pad (32, 34) of a substrate (36), comprising the steps of:

   a) forming an electrically conductive polymerizable precursor (20, 22, 24, 26) on the bond pad (12, 14) of said flip chip (10);

   b) contacting said electrically conductive precursor (20, 22, 24, 26) to said bond pad (32, 34) of said substrate (36), and

   c) while so contacted, polymerizing said precursor (20, 22, 24, 26) to form an electrically conductive interconnection between the bond pad (12, 14) of the flip chip (10) and the bond pad (32, 34) of the substrate (36), characterized in that

   d) in said step a) said precursor (20, 22, 24, 26) is stenciled onto the bond pad (12, 14) of said flip chip (10) to a level extending beyond that of said protecitve layer (18) such that a bump (28, 30) is produced providing for said electrically conductive interconnection.

2. The method of claim 1, wherein prior to step a), an organic protective layer (18) is selectively formed on the surface of the flip chip (10) leaving the bond pad (12, 14) exposed.

3. A method of forming an electrically conductive in-

terconnection between a bond pad (12, 14) of a flip chip (10) and a bond pad (32, 34) of a substrate (36), comprising the steps of:

a) forming an organic protective layer (18) over a surface of the flip chip (10) where the bond pad (12, 14) is located;

b) forming an electrically conductive polymerizable precursor (20, 22, 24, 26) on the bond pad (12, 14) of said flip chip (10);

c) contacting said electrically conductive precursor (20, 22, 24, 26) to said bond pad (32, 34) of said substrate (36), and

d) while so contacted, polymerizing said precursor (20, 22, 24, 26) to form an electrically conductive interconnection between the bond pad (12, 14) of the flip chip (10) and the bond pad (32, 34) of the substrate (36), characterized in that

e) in said step a) said protective layer (18) is selectively formed on said flip chip (10) such that said bond pad (12, 14) remains exposed, and

f) in said step b) said precursor (20, 22, 24, 26) is formed onto the bond pad (12, 14) of said flip chip (10) to a level extending beyond that of said protective layer (18) such that a bump (28, 30) is produced providing for said electrically conductive interconnection.

4. The method of claim 3, wherein said electrically conductive polymerizable precursor (20, 22, 24, 26) is stenciled onto the bond pad (12,14) of said flip chip.

5. The method of any of the preceding claims 2-4, wherein said organic protective layer (18) is formed by screen printing, stenciling or spin-etching.

6. The method of any of the preceding claims 2-5, wherein said organic protective layer (18) is a dielectric polymer.

7. The method of any of the preceding claims, wherein said electrically conductive polymerizable precursor (20, 22, 24, 26) is polymerized to form said electrically conductive bump (28, 30) prior to contacting said bump (28, 30) to the bond pad (32, 34) of the substrate (36).

8. The method of any of the preceding claims 2-7, wherein said organic protective layer (18) defines the area for forming the electrically conductive polymerizable precursor (20, 22, 24, 26) on said flip chip (10).

9. The method of any of the preceding claims wherein said formation of said polymerizable precursor (20, 22, 24, 26) comprises the steps of:

a) forming a first layer (20, 22) of an electrically conductive polymerizable precursor on the bond pad (12, 14) of the flip chip (10);

b) forming a second layer (24, 26) of an electrically conductive polymerizable precursor over the first layer, the second layer and the first layer together forming said bump (28, 30).

10. The method of claim 9 wherein said first layer (20, 22) is formed substantially flush with said protective layer (18).

11. The method of any of the preceding claims 7 through 10, as far as they refer back to claim 7, further comprising the step of forming an electrically conductive adhesive (38, 40) on the substrate bond pad (32, 34) to allow an electrically conductive interconnection between the bond pad (12, 14) of the flip chip (10) and the bond pad (32, 34) of the substrate.

12. The method of claim 11, wherein said electrically conductive adhesive (38, 40) is stenciled onto the substrate bond pad (32, 34).

13. The method of claim 11, wherein said electrically conductive adhesive (38, 40) is deposited onto said bond pad (32, 34) of said substrate (36).

14. The method of any of the preceding claims 9 through 13, further comprising the steps of:

a) drying said first layer (20, 22) after formation;

b) drying said second layer (24, 26) after formation.

15. The method of claim 9, further comprising the steps of:

a) polymerizing said first layer (20, 22) after formation to form an electrically conductive polymer;

b) polymerizing said second layer (24, 26) after formation to form said electrically conductive bump (28, 30) on the bond pad (12, 14) of the flip chip (10);

c) applying an electrically conductive adhesive

(38, 40) to said substrate bond pad (32, 34), and

d) contacting said adhesive (38, 40) to said electrically conductive bump (28, 30) to form said electrically conductive interconnection between said bond pad (12, 14) of the flip chip (10) and said bond pad (32, 34) of said substrate (36).

16. The method of claim 15, further including the step of polymerizing the electrically conductive adhesive (38, 40) while the electrically conductive adhesive is in contact with the bond pad (32, 34) of the substrate (36).

17. The method of any of the preceding claims, wherein said electrically conductive polymerizable precursor (20, 22, 24, 26) includes a thermoset polymer, a B-stage polymer a thermoplastiv polymer, or any monomer or polymer which, upon polymerization or upon further polymerization, is electrically conductive or which can support an electrically conductive material.

18. A bumped flip chip comprising:

a) a flip chip (10);

b) an organic protective coating (18) over a surface of the flip chip (10); and

c) an electrically conductive polymer bump (20, 22).

19. An electrical circuit comprising:

a) a substrate (36) having a bond pad (32, 34);

b) a flip chip (10) having an organic protective coating (18) and a bond pad (12, 14);

c) an electrically conductive polymer (20, 22, 24, 26) interconnect between the bond pad (32, 34) of the substrate (36) and the bond pad (12, 14) of the flip chip (10).

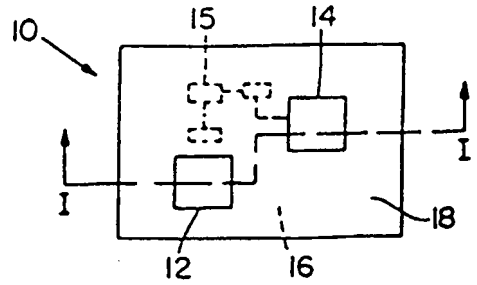


Fig. 1

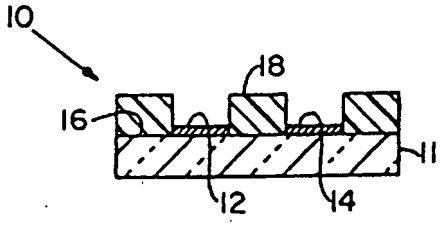


Fig. 2

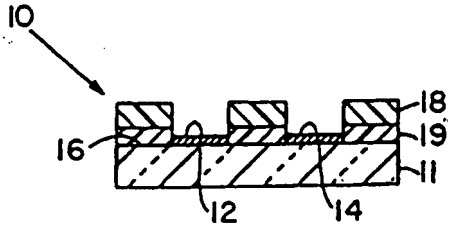


Fig. 3

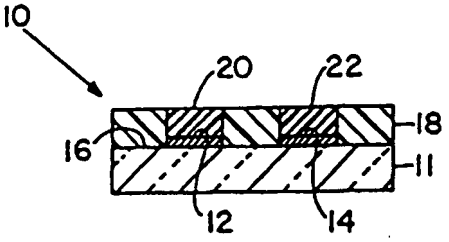


Fig. 4

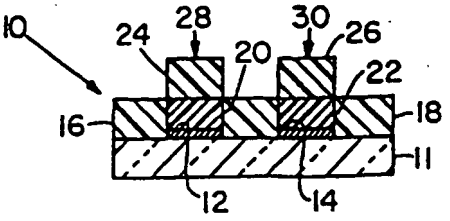


Fig. 5

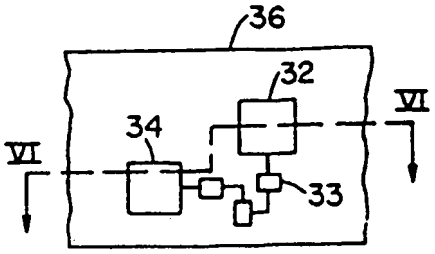


Fig. 6

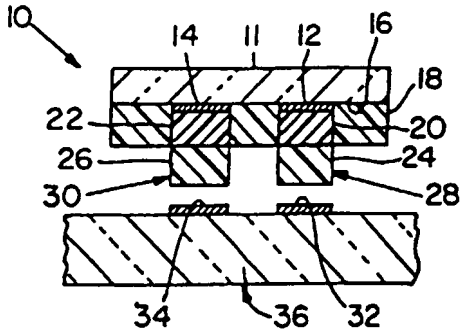


Fig. 7

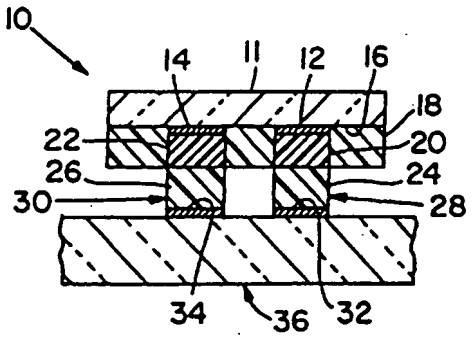


Fig. 8

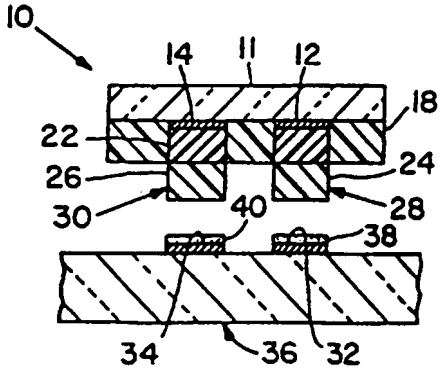


Fig. 9

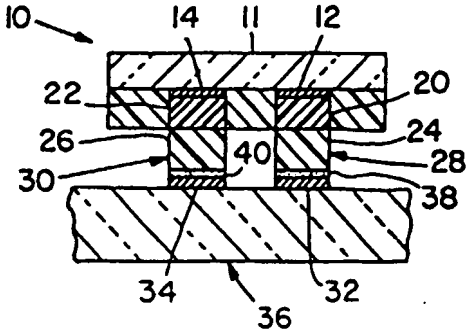
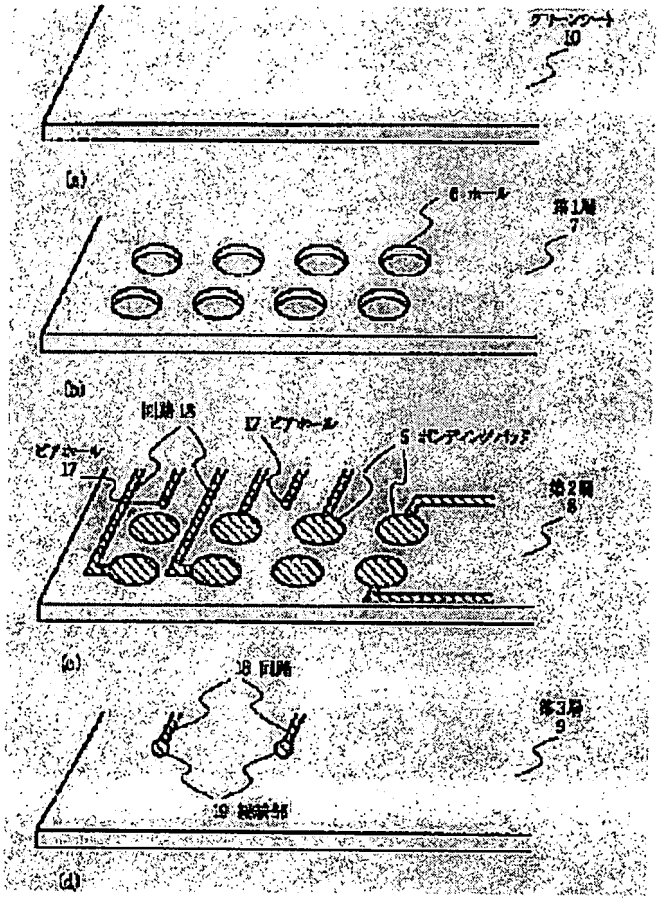


Fig. 10

1) Family number: 12550537 (JP7169873 A2) © PatBase

Title: MULTI-LAYER BOARD AND MANUFACTURE THEREOF

Abstract:
Source: JP7169873A2 PURPOSE: To improve productivity by a method wherein a bonding pad where a bump electrode is electrically connected to a lower layer is provided on a multi-layer board, a hole is provided on the lower layer corresponding to the bonding pad to easily allow the positioning between the semiconductor a board with substantially simplified manufacturing process. CONSTITUTION: Green sheet 10 is punched to form a hole 6 and to obtain a first layer board 7. Then, a circuit pattern 18 is formed on the second layer board 8. A bonding pad is provided on the section contacting with the solder bump of the semiconductor. Moreover, a pier hole 17 electrically connecting to the third layer board 9 is provided on the end section of the circuit pattern 18, and a connecting section 19 is provided on the position corresponding to the via hole 17 on the second layer board. Then, the first - third layer boards 7-9 are piled and sintered to obtain a multi-layered board.



International class (IPC 8): H05K1/03 H05K3/40 H05K3/46 (Advanced/Non-invention); H05K1/03 H05K3/40 H05K3/46 (Core/Non-invention)
International class (IPC 1-7): H01L21/60 H01L23/12 H05K1/18 H05K3/34 H05K3/46

Family:	Publication number	Publication date	Application number	Application date
	JP2606110 B2	19970430	JP19930314762	19931215
	JP7169873 A2	19950704	JP19930314762	19931215

Priority: JP19930314762 19931215

Assignee(s): (std): NIPPON ELECTRIC CO

Inventor(s): OGISO MICHINORI